

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "VDD_CORE" represents connection to the +1.1V power buss.
2. The netname "VDD_MPU" represents connection to the +1.2V power buss
3. The netname "VDD_1V8" represents connection to the +1.8V power busses
4. The netname "VDD_PLL" represents connection to the +1.8V power busses
5. The netname "VDDS_DDR" represents connection to the +1.5V power buss.
6. The netname "DDR_VREF" represents connection to the +0.75V power buss
7. The netname "VDD_PHYA" represents connection to the +3.3V power buss.
8. The netname "P12V_SUPPLY" represents connection to the +12V power buss.
9. The netname "P5P0V" represents connection to the +5.0V power buss.
10. The netname "P5V" represents connection to the +5.0V power buss.
11. The netname "VDD_3V3AUX" represents connection to the +3.3V power buss.
12. The netname "P1P2V" represents connection to the +1.2V power buss.
13. The netname "P1P9V" represents connection to the +1.9V power buss.
14. The netname "P2P5V" represents connection to the +2.5V power buss.
15. The netname "P3P3V" represents connection to the +3.3V power buss.
16. The netname "VOFFSET" represents connection to the +8.5V power buss.
17. The netname "VBIAS" represents connection to the +16.0V power buss.
18. The netname "VRESET" represents connection to the -10.0V power buss
19. The netname "GND" and "DGND" represents connection to the ground plane.
20. A "Z" suffix on a signal name indicates an active low signal.
21. All resistor values are in ohms.
22. All capacitor values in microfarads unless otherwise specified.
23. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.



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		ENGR Eric Pruett					
		APVD Joe Siddall					
		MFG		TITLE ESD, NIRscan Spectro Board			
2513464	0314CP	QA					
NEXT ASSY	USED ON			A3	DRAWING NO 2513462	REV D	
APPLICATION		SW Allegro Design Entry 16.6					SCALE

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
-	Draft Release	09/23/2013	HPC
A	ECO 2136066: REV A Release	11/01/2013	HPC
B	ECO 2138776: REV B	01/06/2014	GSW
C	ECO 2139942: REV C	02/13/2014	HPC
D	ECO 2140608: REV D	03/14/2014	HPC

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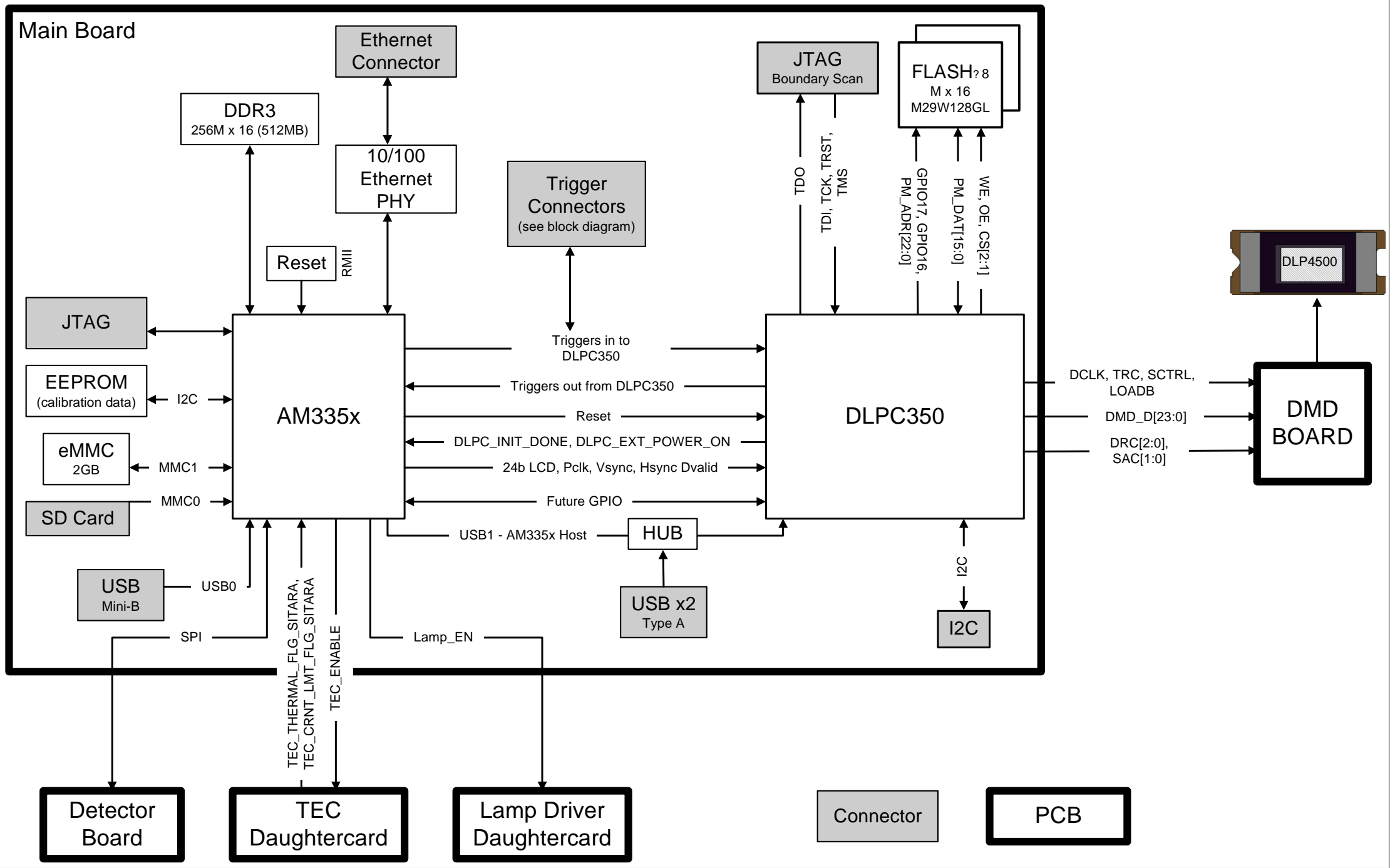
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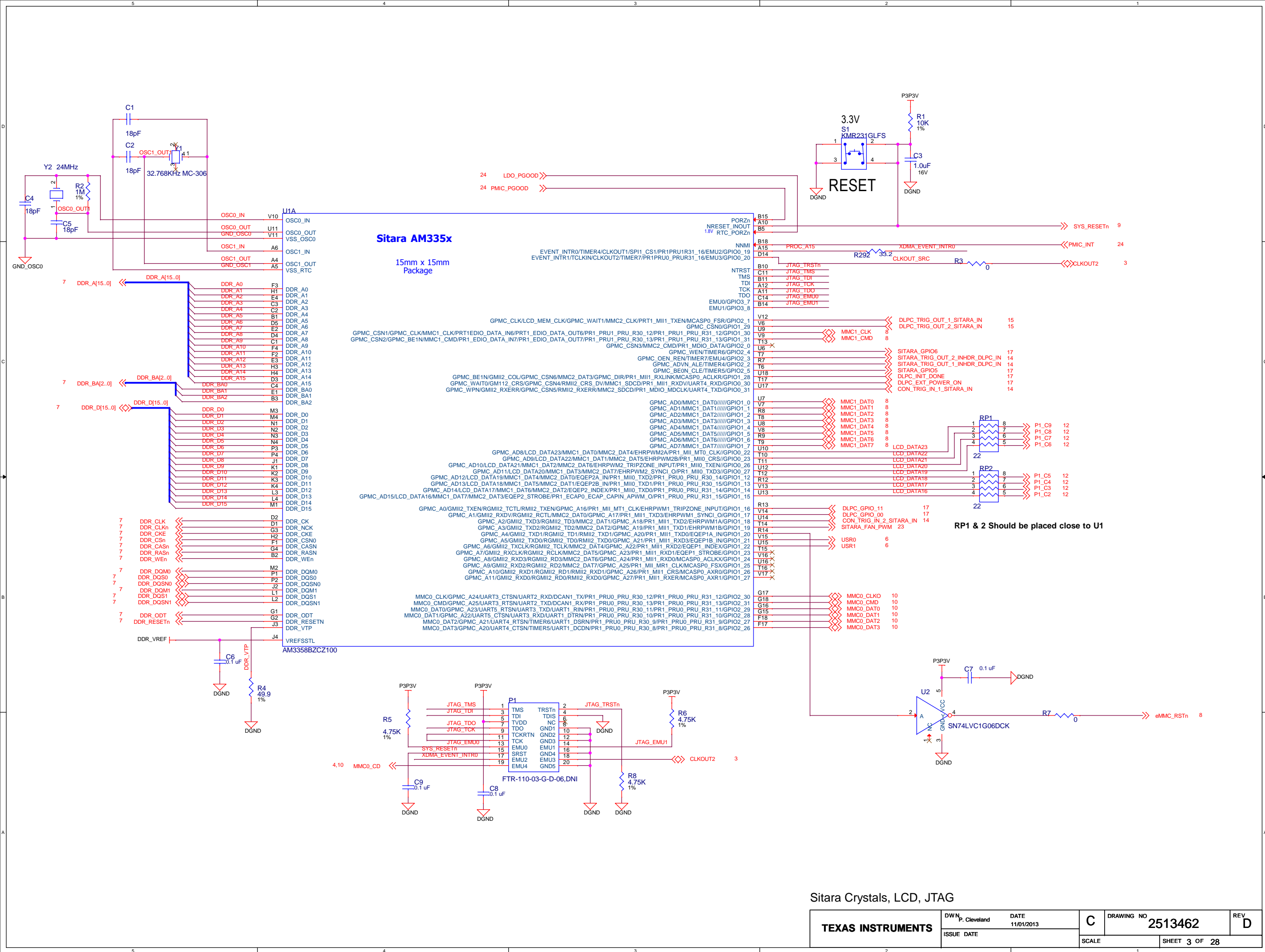
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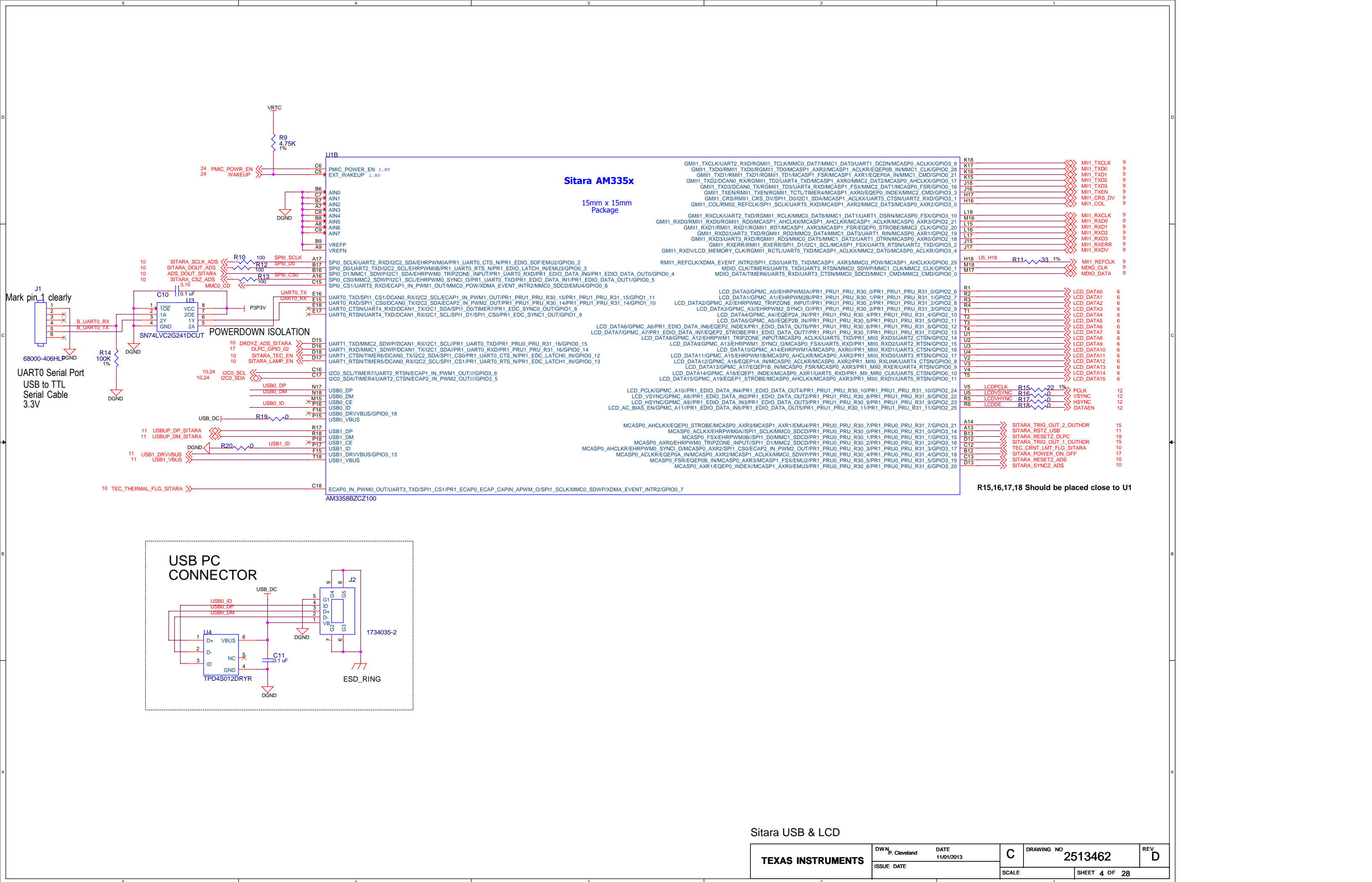
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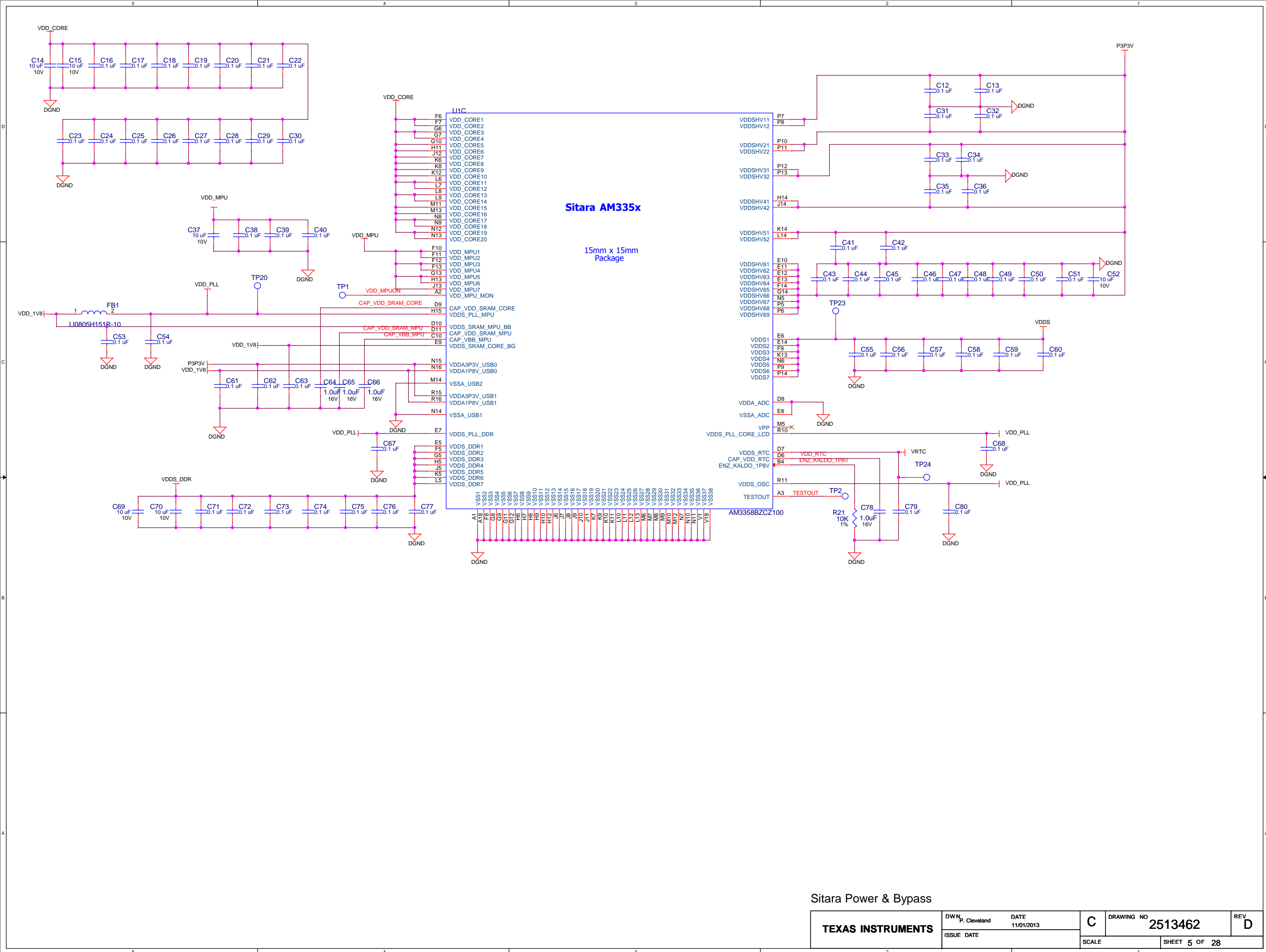


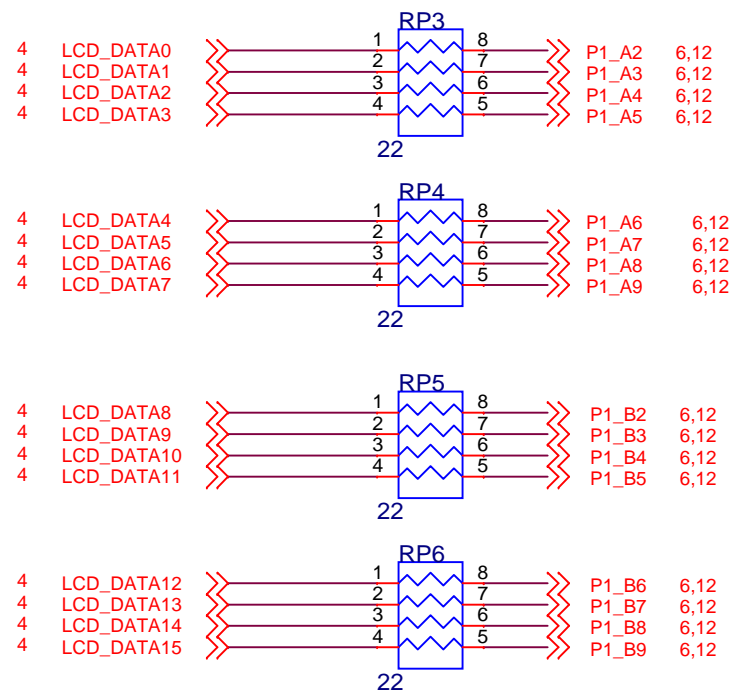
ELECTRONICS BLOCK DIAGRAM

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	ISSUE DATE					
				SCALE		SHEET 2 OF 28

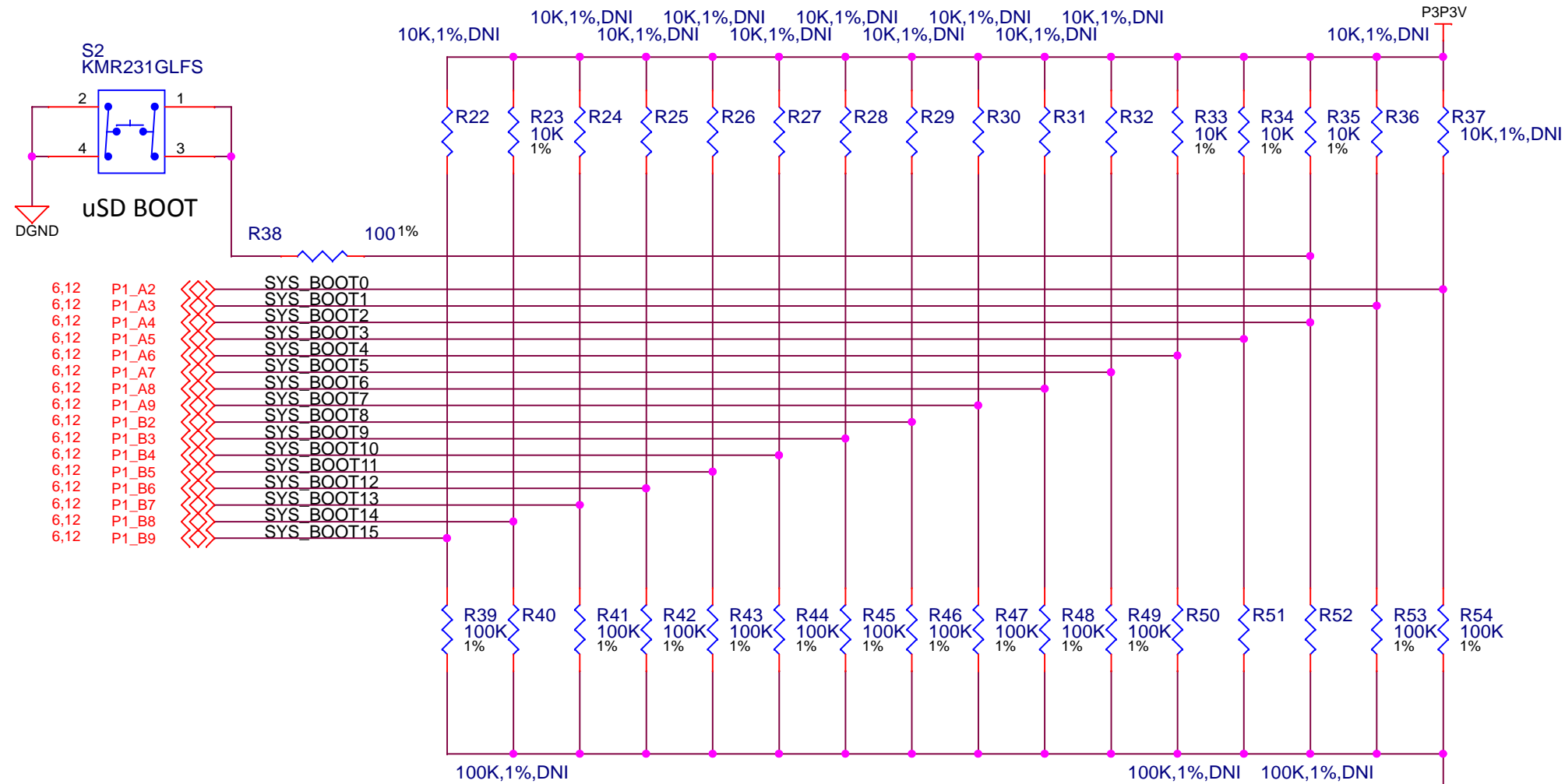






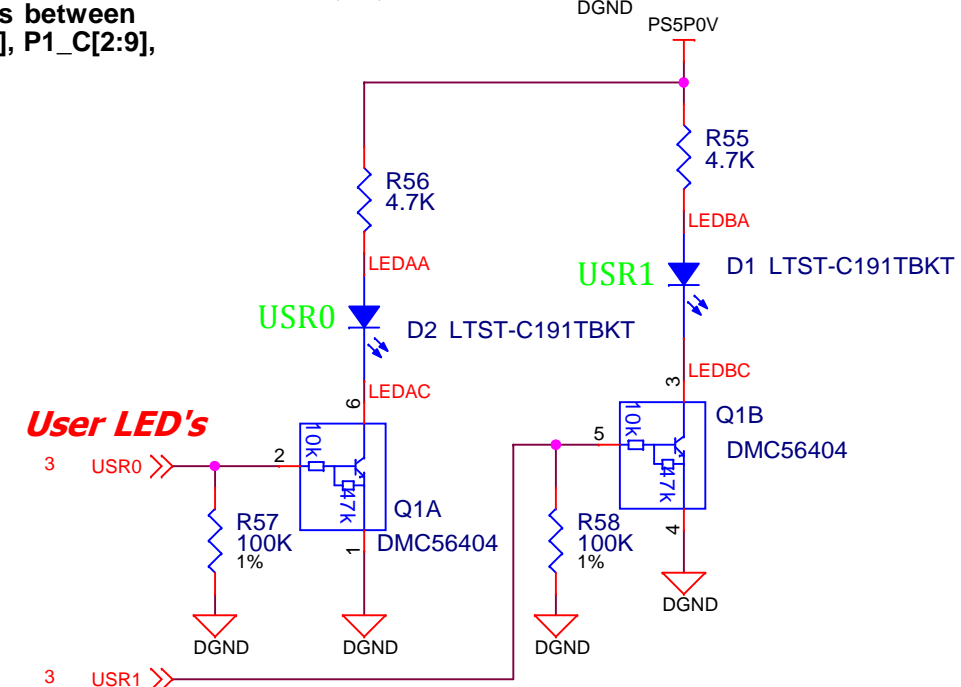


RP3,4,5,6 Should be placed close to U1

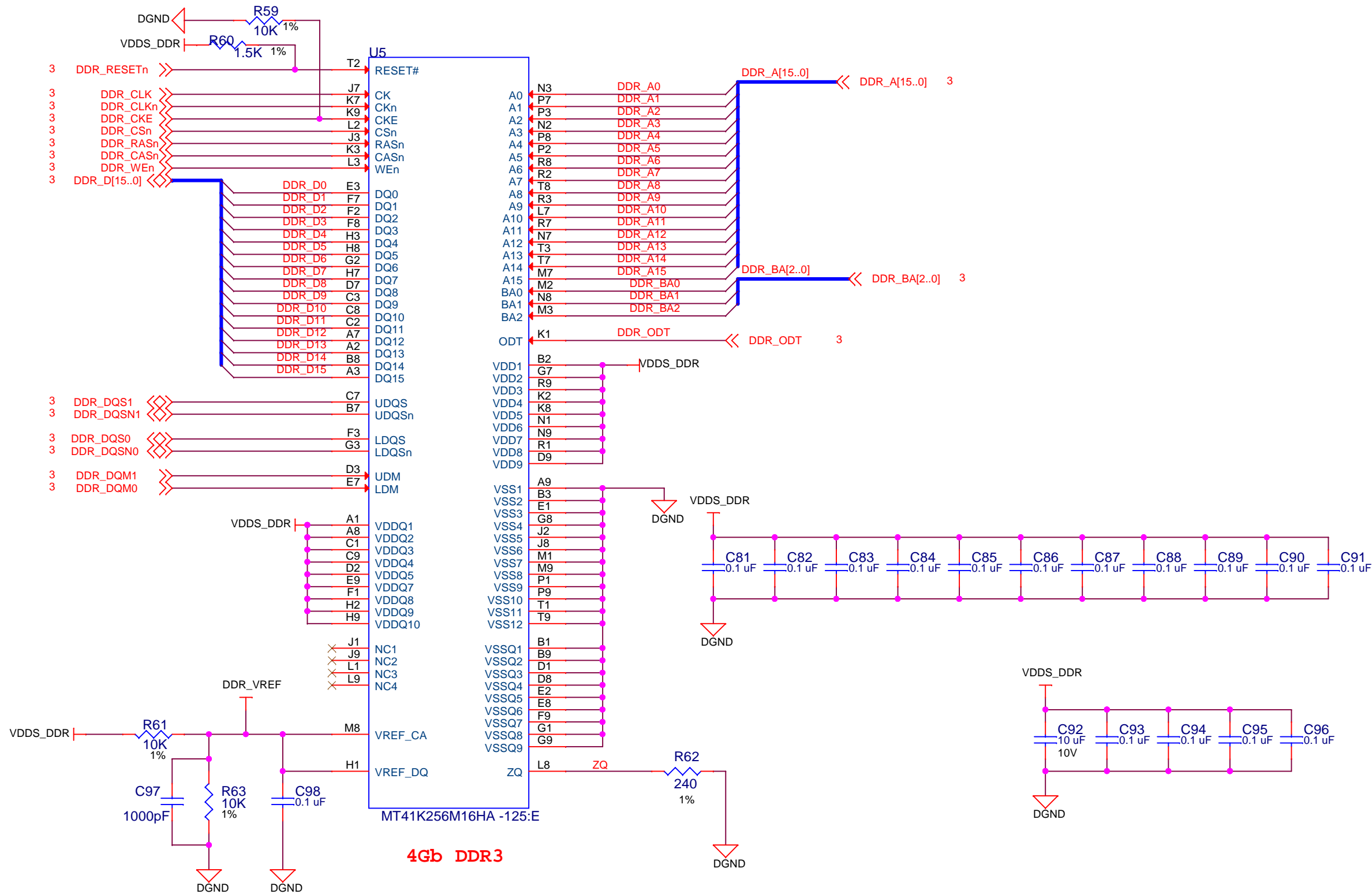


R22 -> R54; Minimize lead lengths between resistors and P1_A[2:9], P1_B[2:9], P1_C[2:9],

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5] 1	UART0

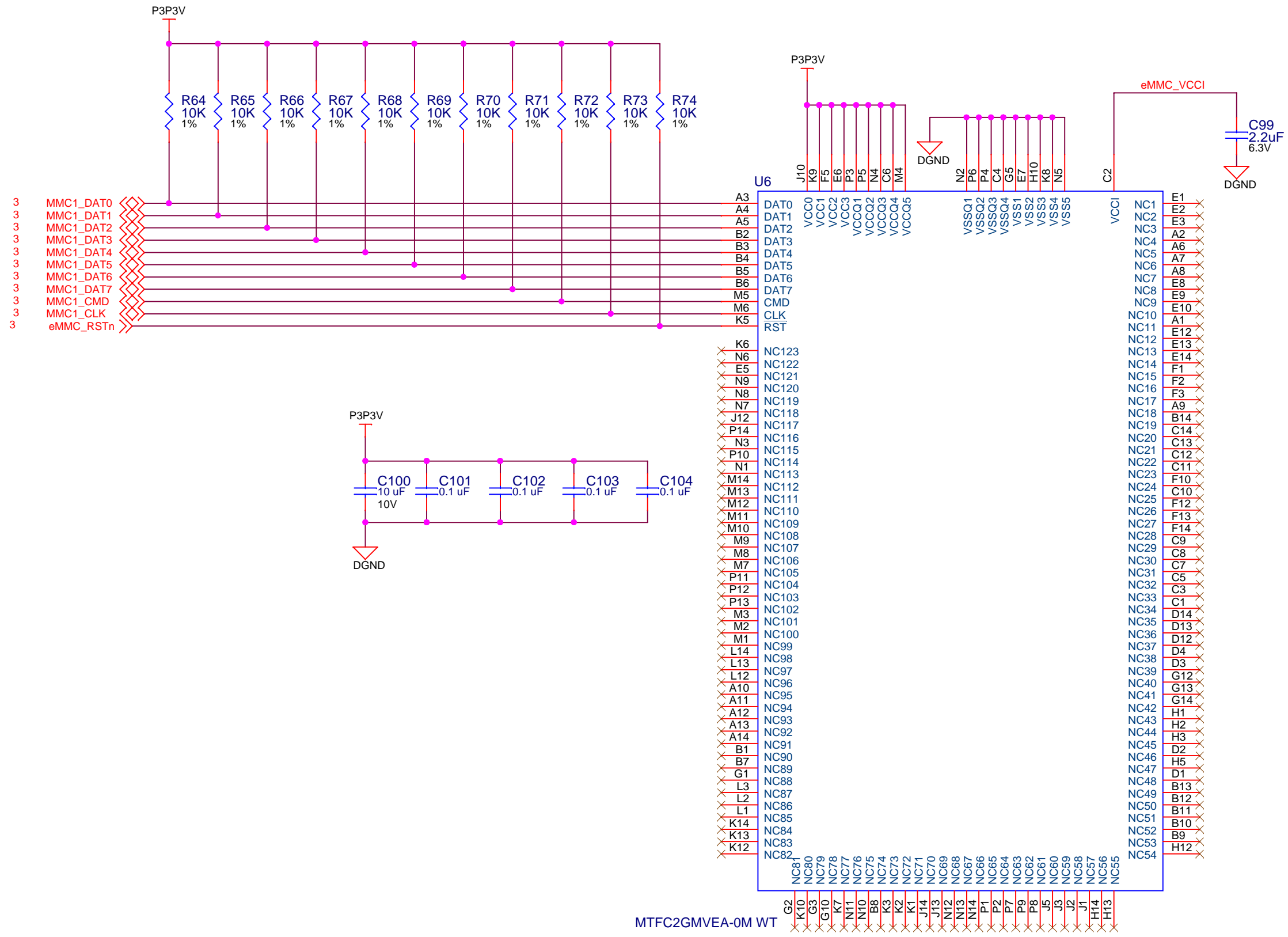


Boot configuration, User LEDs



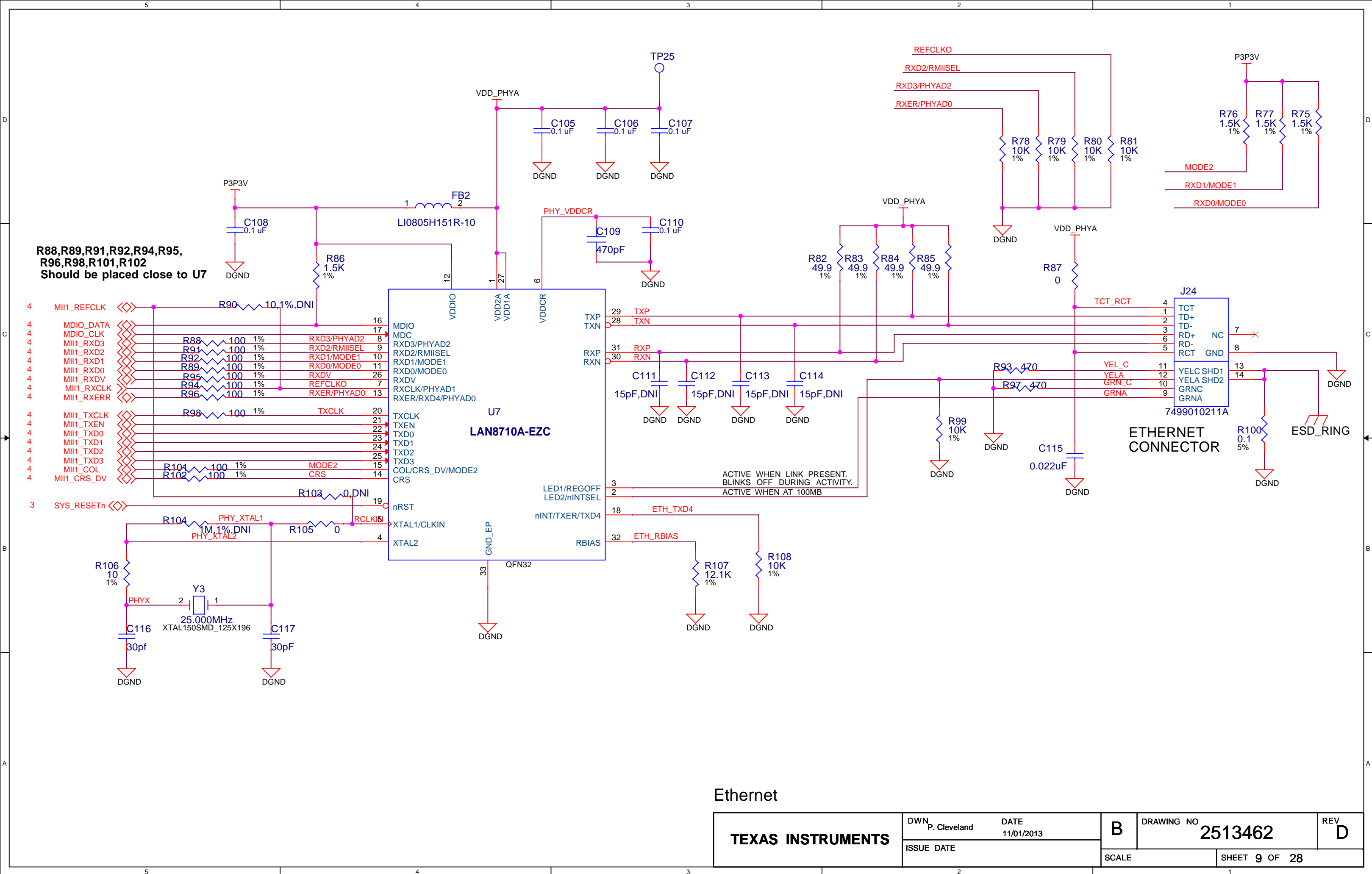
DDR3L SDRAM

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	ISSUE DATE			SCALE		SHEET 7 OF 28

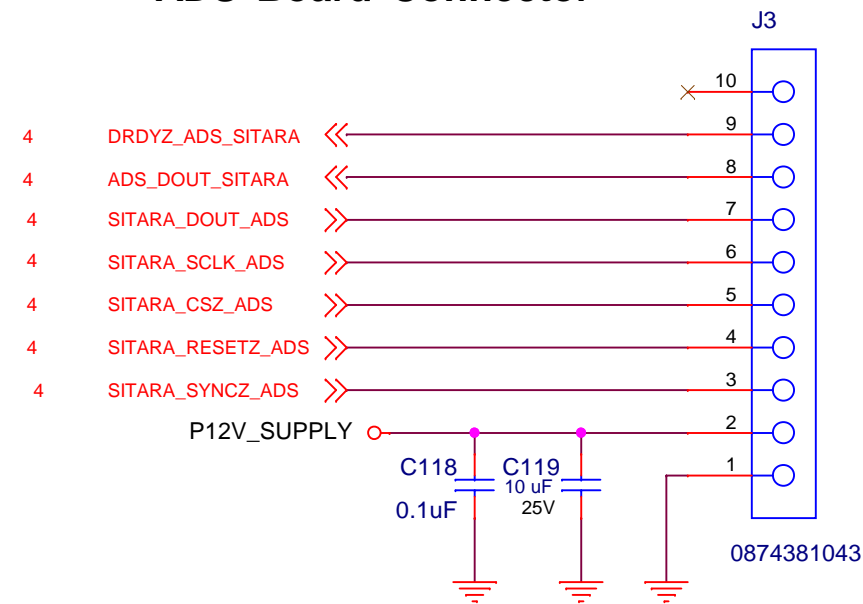


eMCC Flash

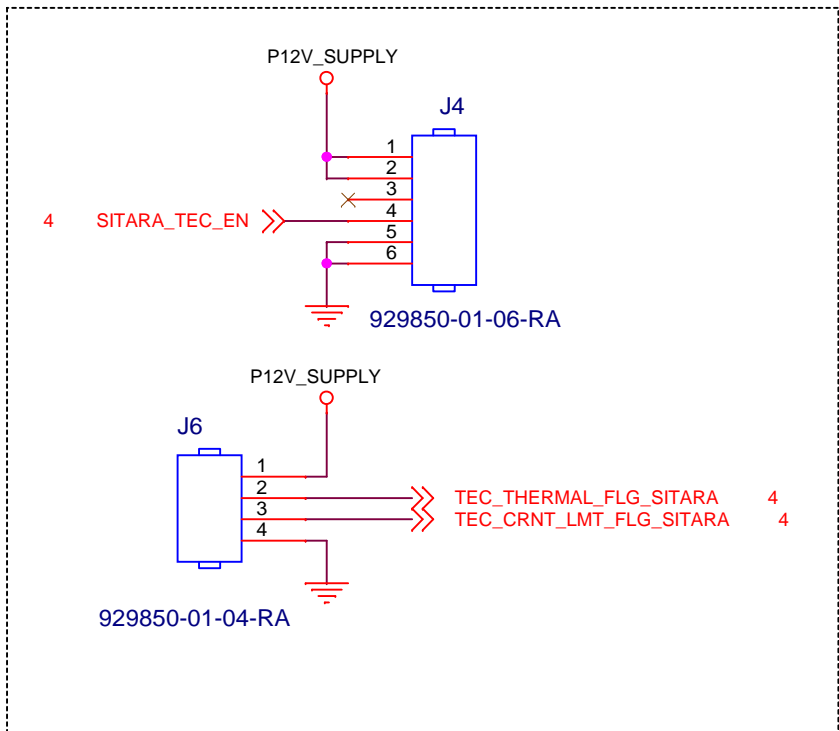
TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	B	DRAWING NO 2513462		REV D
	ISSUE DATE					
				SCALE		SHEET 8 OF 28



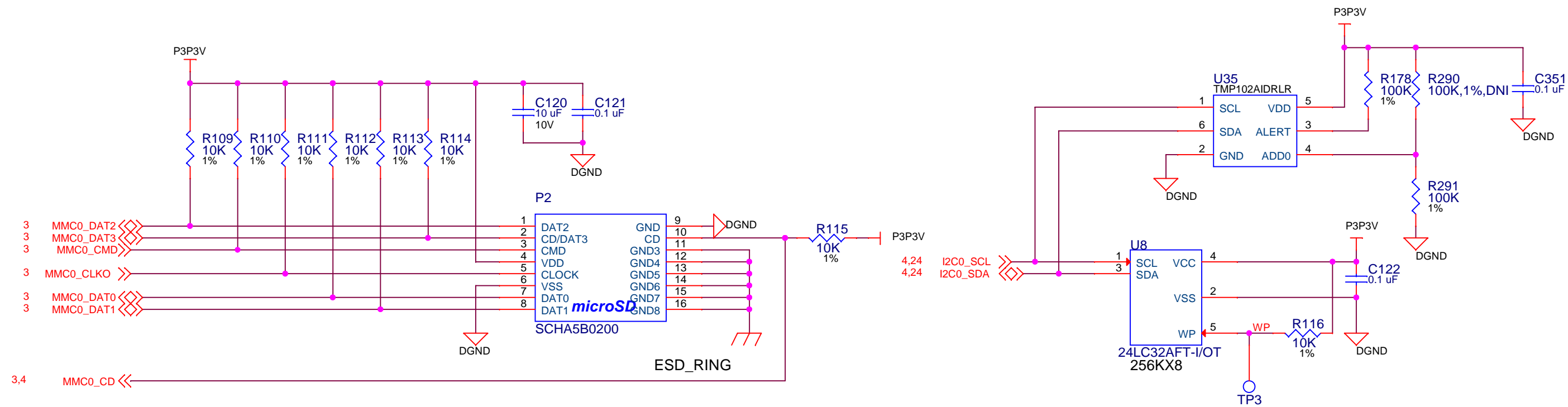
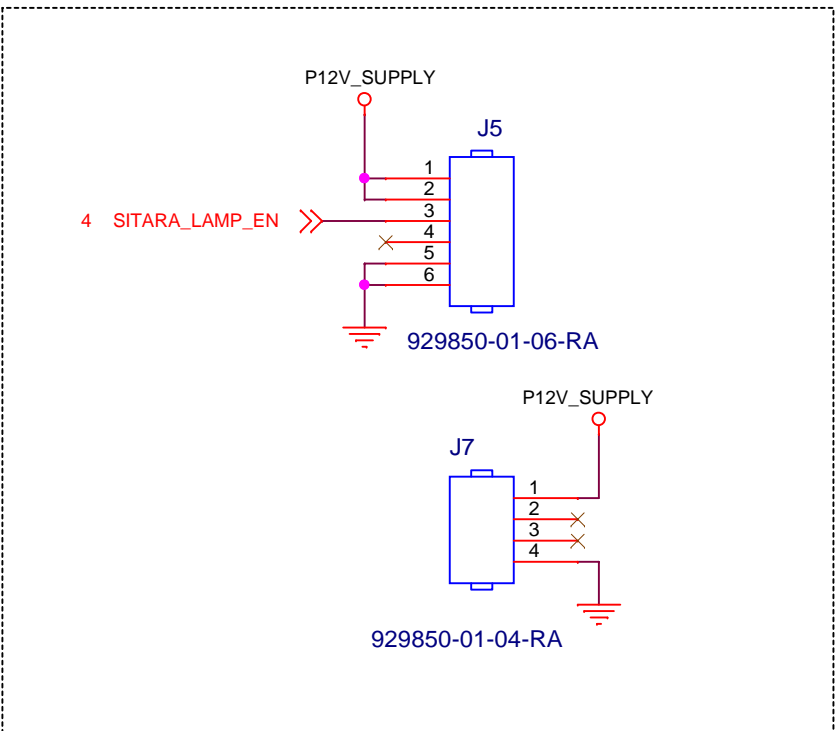
ADS Board Connector



TEC Daughter Board Connectors

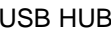


Lamp Driver Daughter Board Connectors



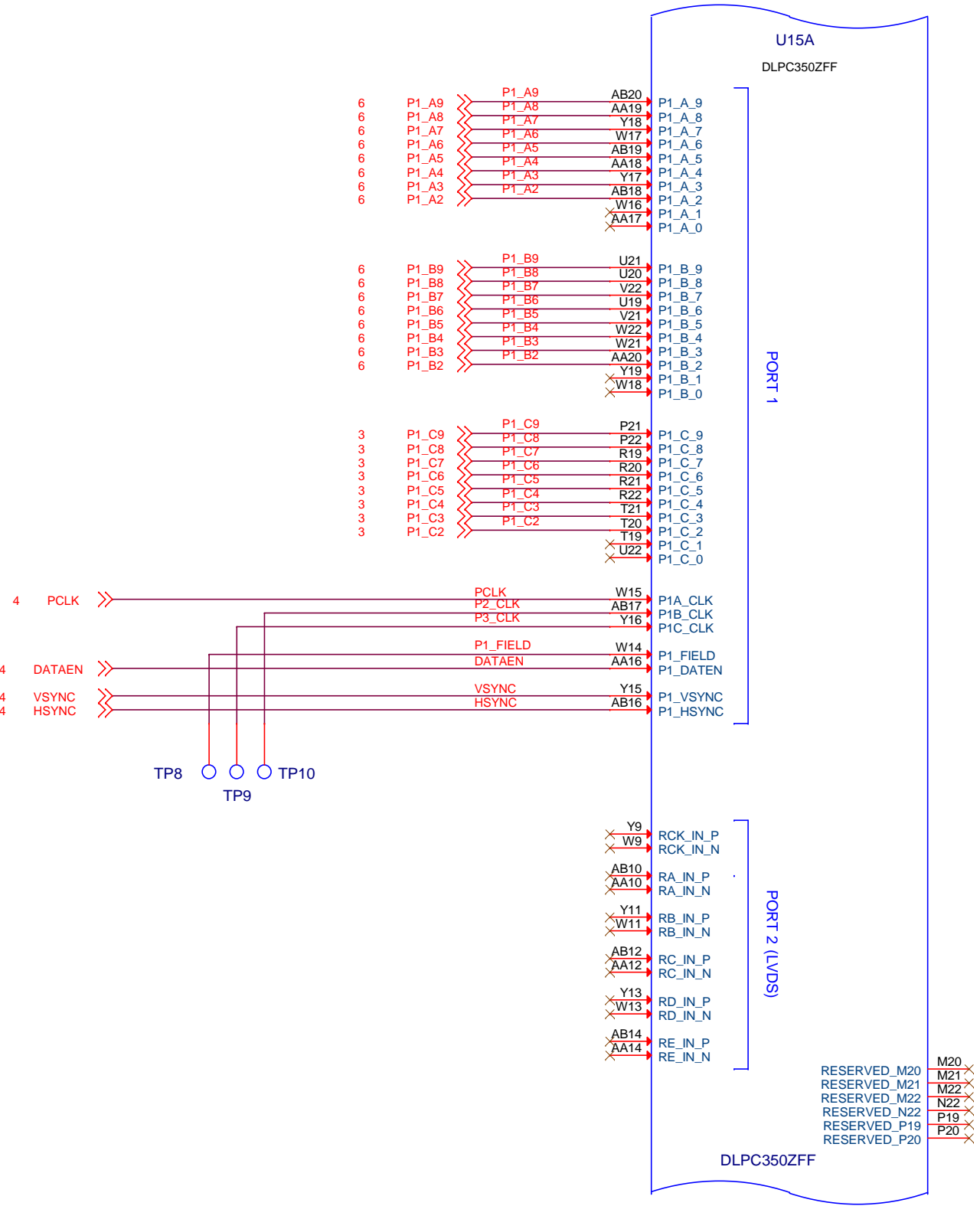
Temperature Sensor, uSD, Detector, & Daughter connectors

TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	B	DRAWING NO 2513462		REV D
	ISSUE DATE			SCALE	SHEET 10 OF 28	



NOTE:
The input data channels can be configured to optimize board layout for each port.
Bitwise reordering is not supported.

For example, Y data could be connected to Port A, B, or C.
Port configuration is handled in the API Software.



Front End Interface

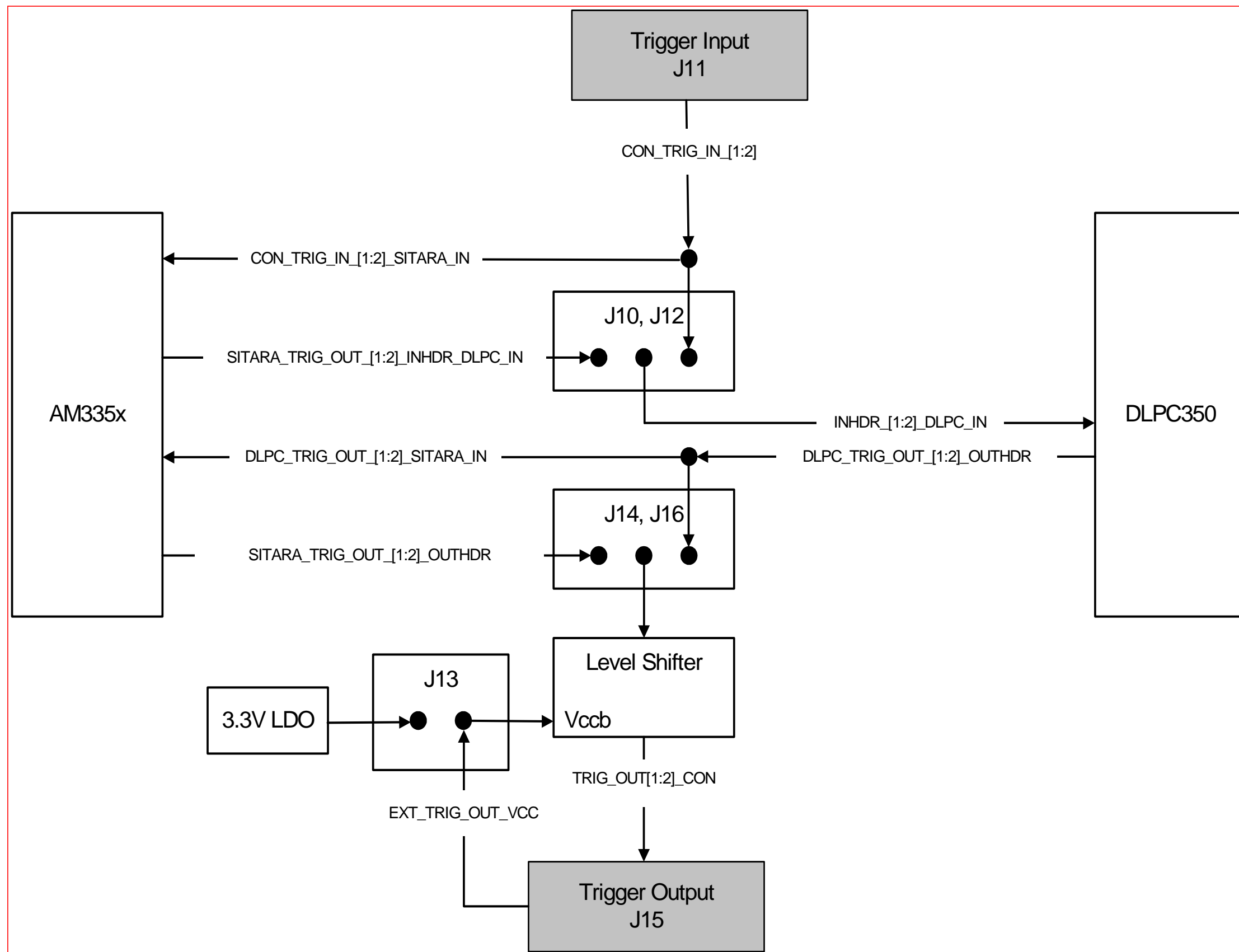
TEXAS INSTRUMENTS

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P. Cleveland
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A3
DRAWING NO
2513462

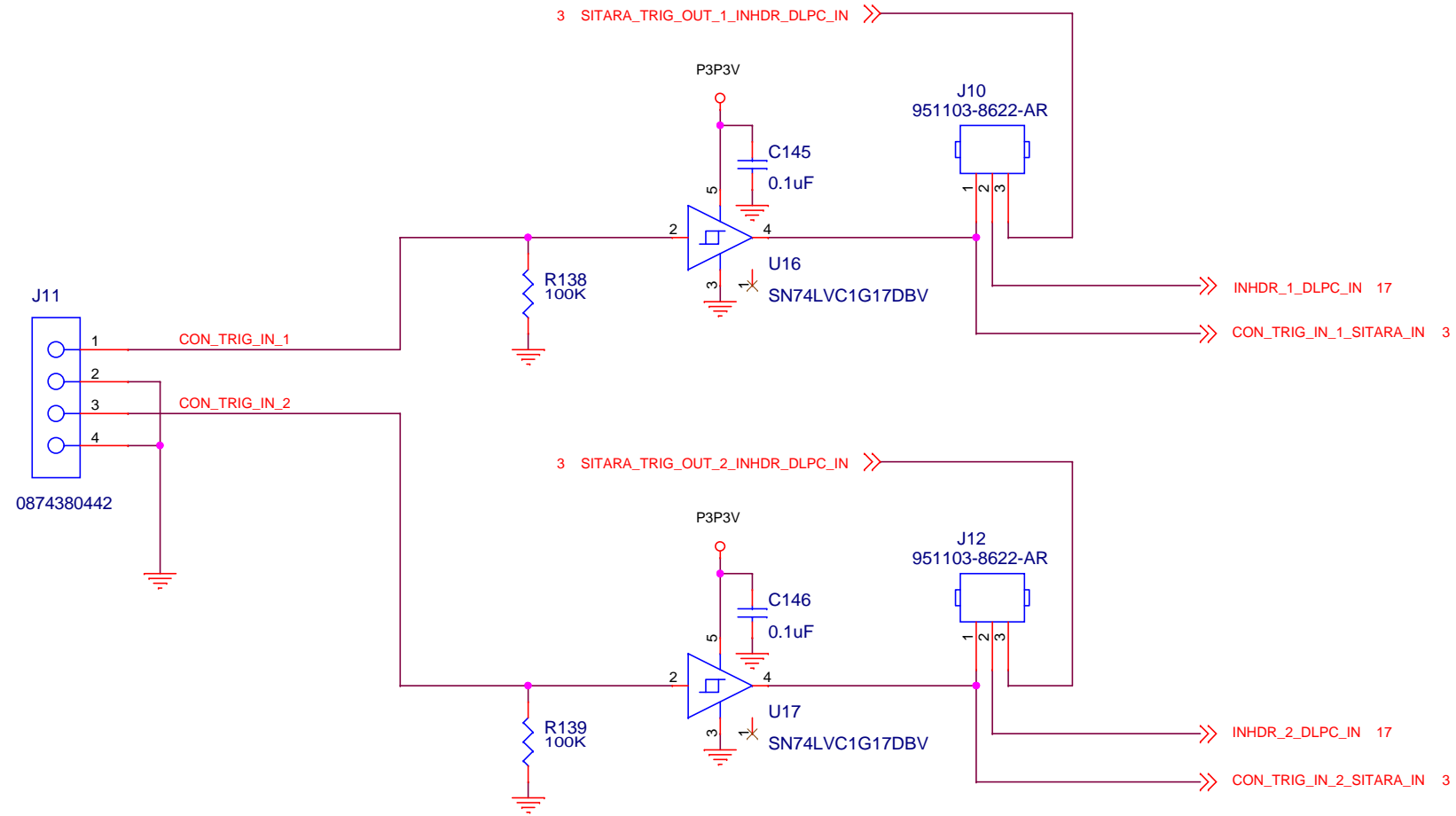
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SHEET 12 OF 28



TRIGGER BLOCK DIAGRAM

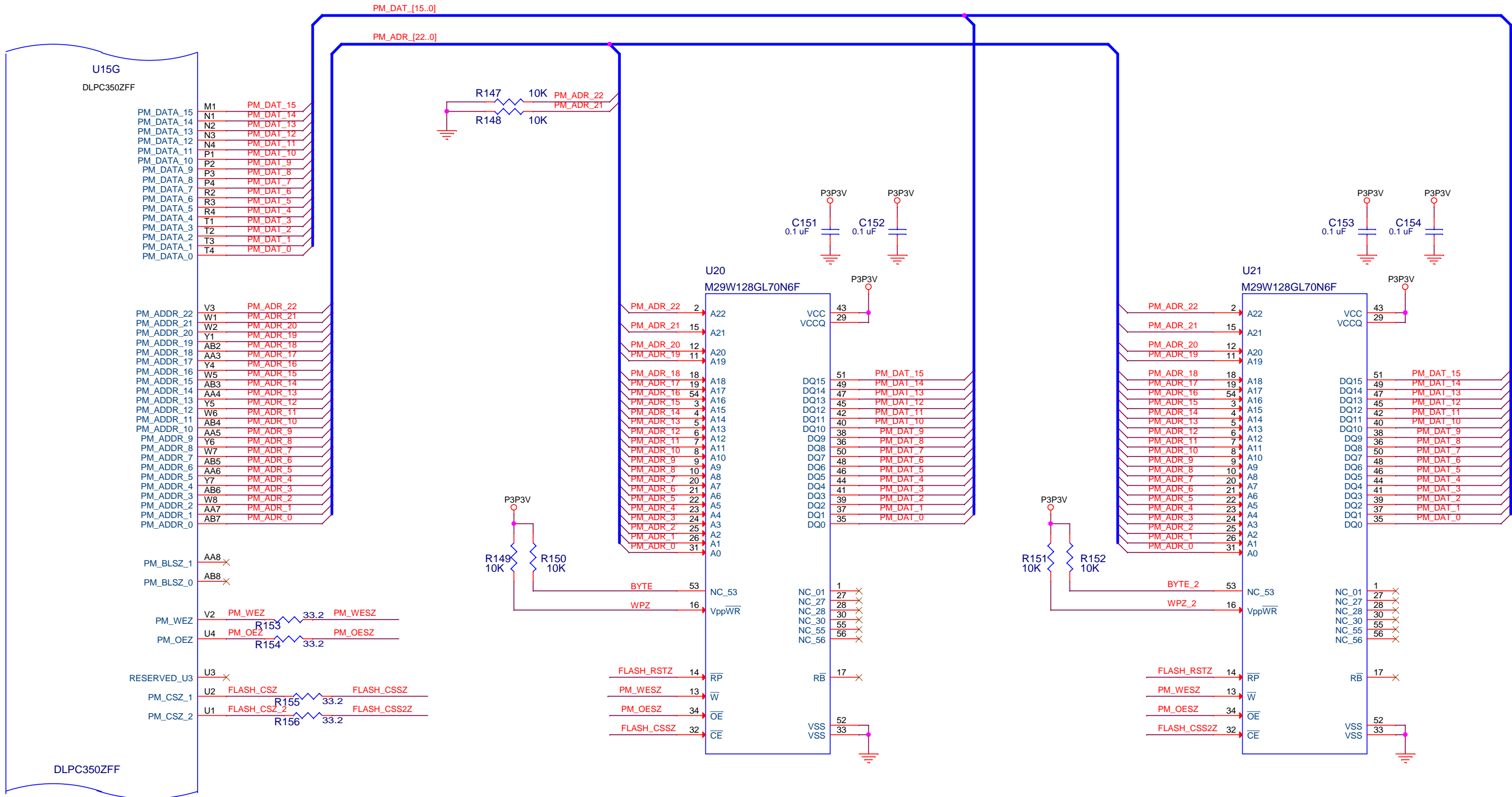
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	ISSUE DATE					
				SCALE		SHEET 13 OF 28



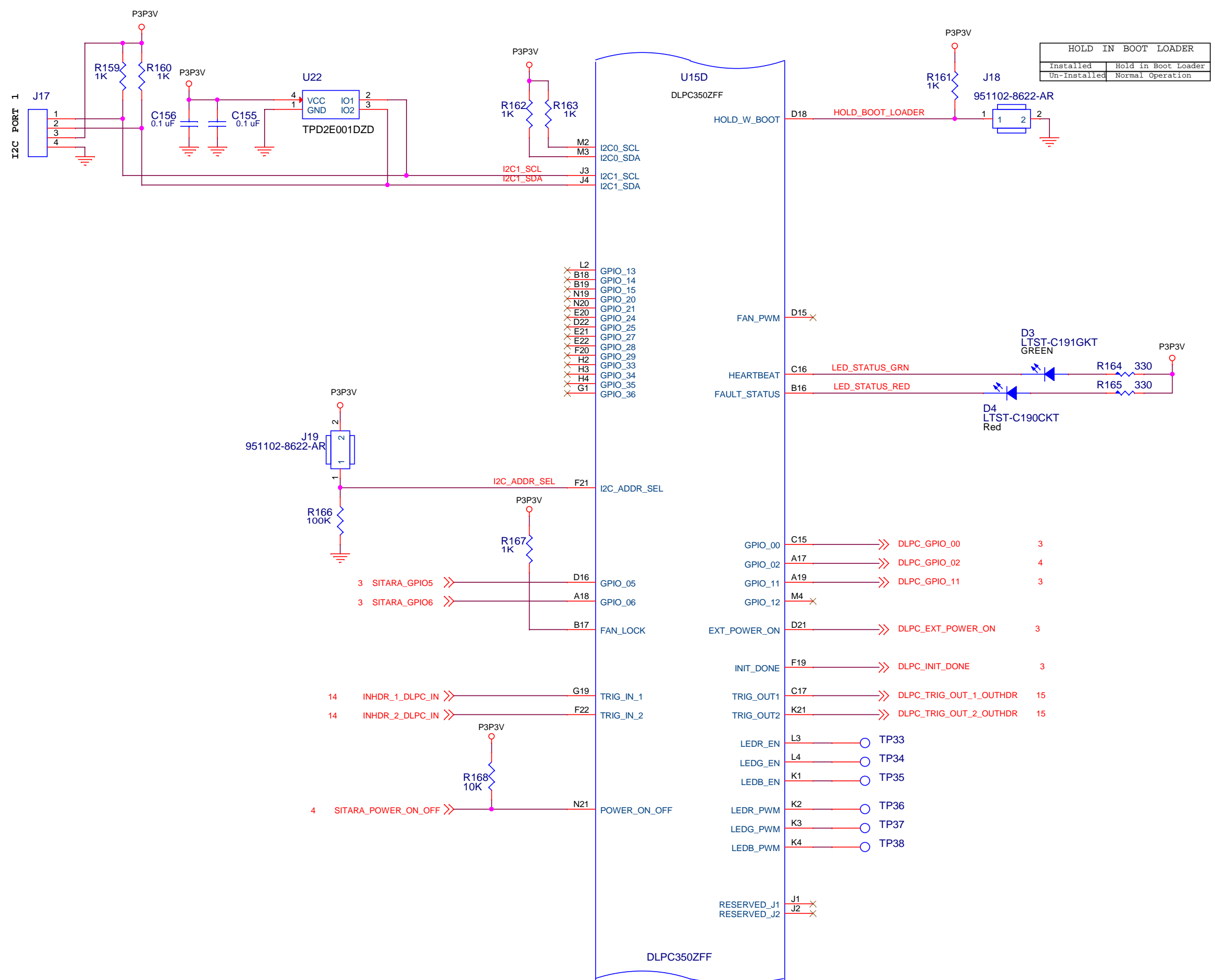
Trigger Input

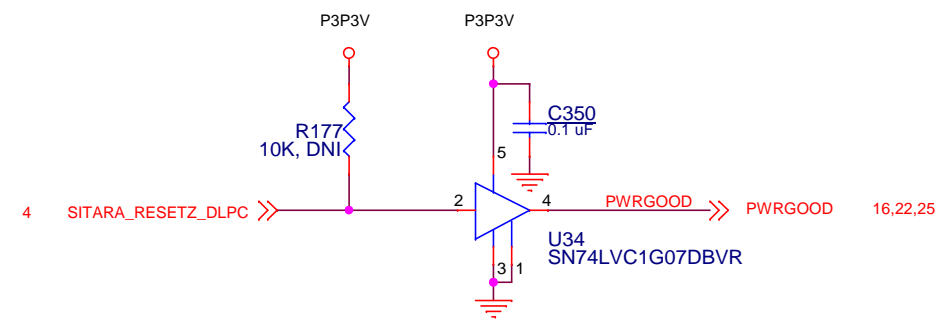
TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	A3	DRAWING NO 2513462		REV D
	ISSUE DATE					
				SCALE		SHEET 14 OF 28



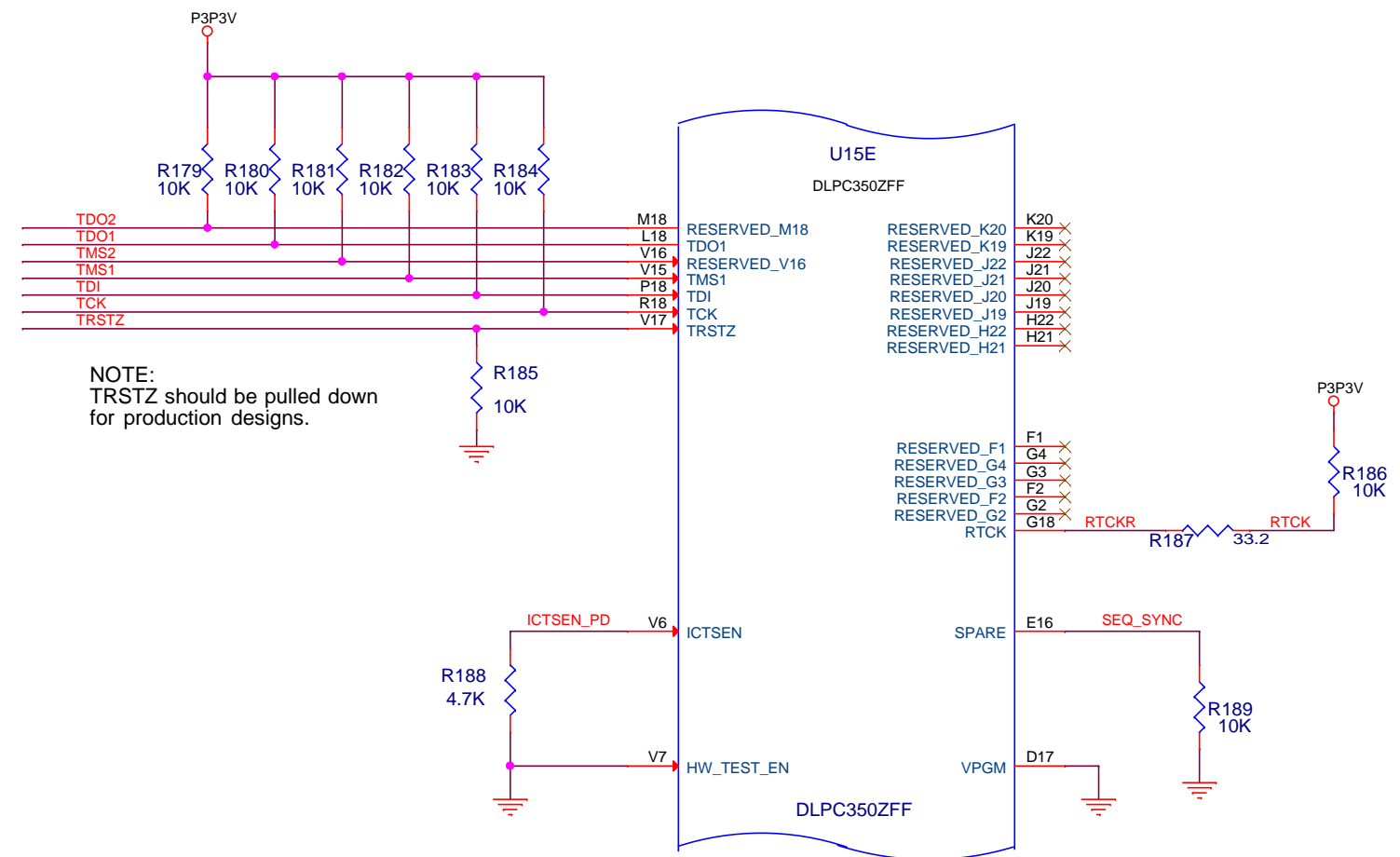
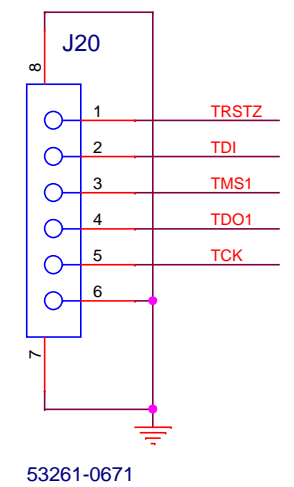


Flash Memory Interface



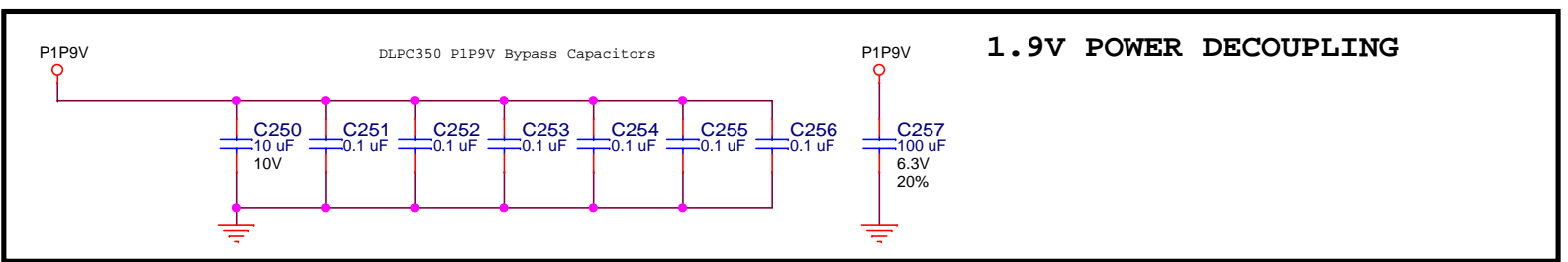
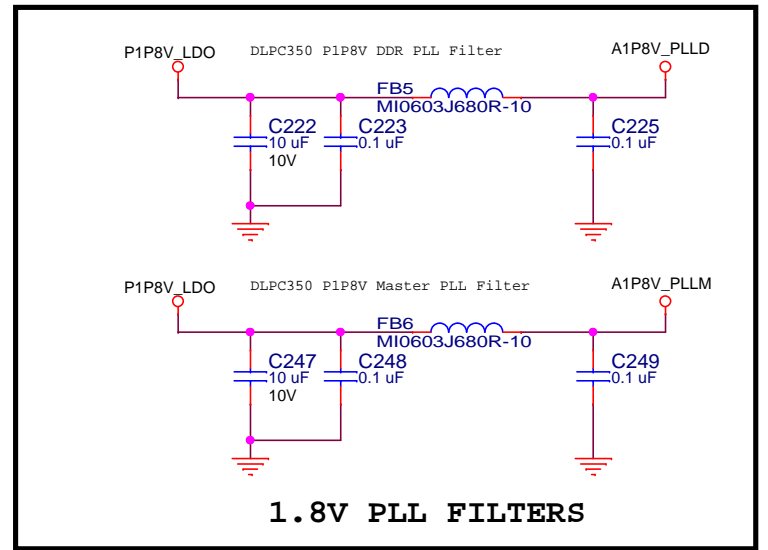
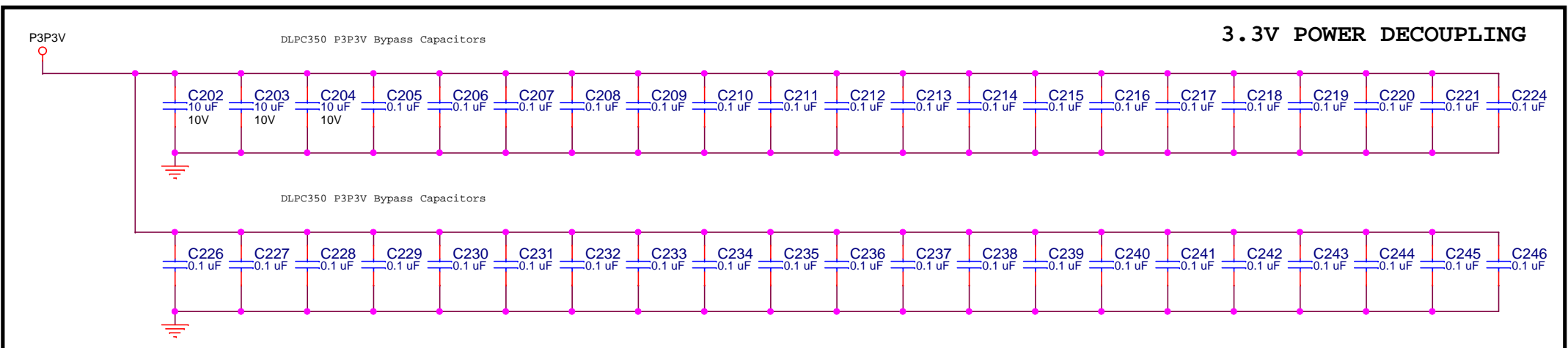
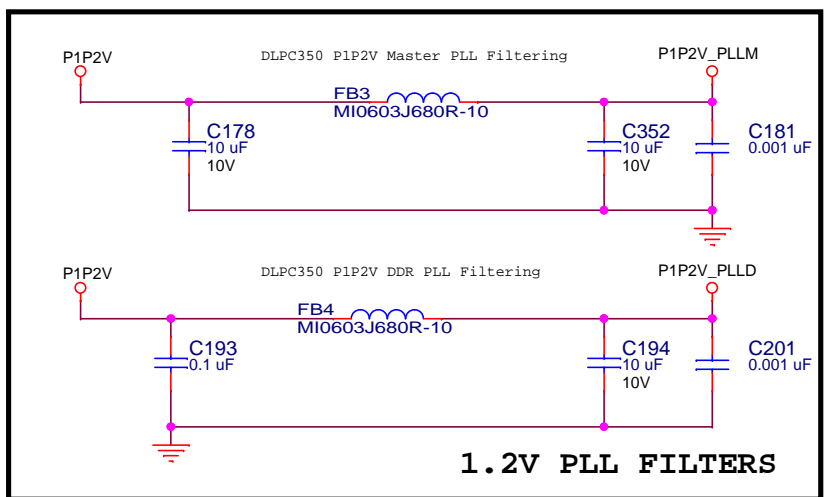
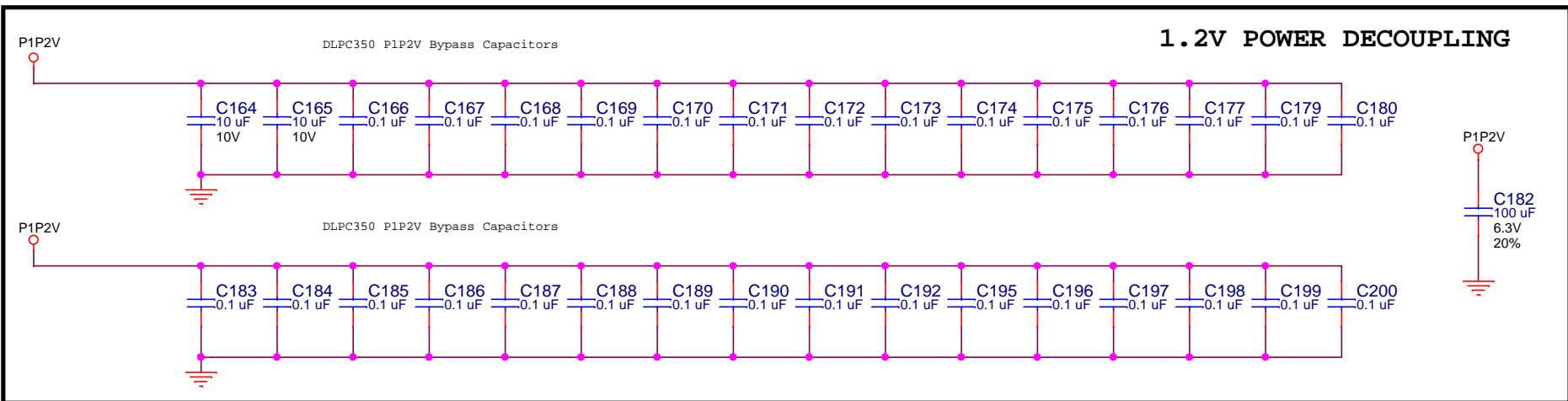
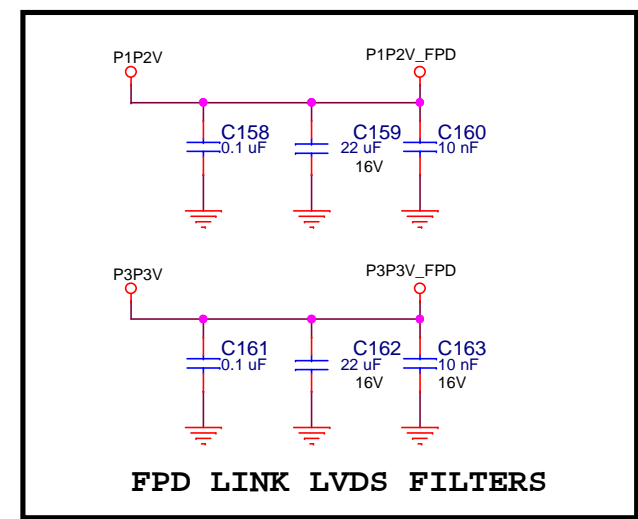
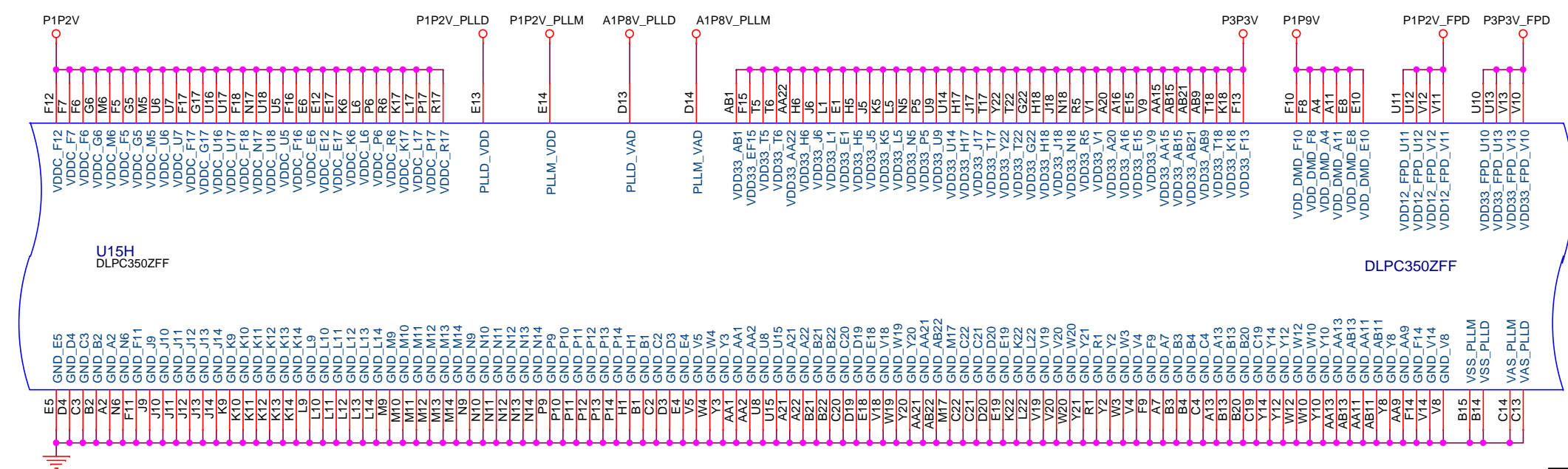


JTAG BOUNDARY SCAN



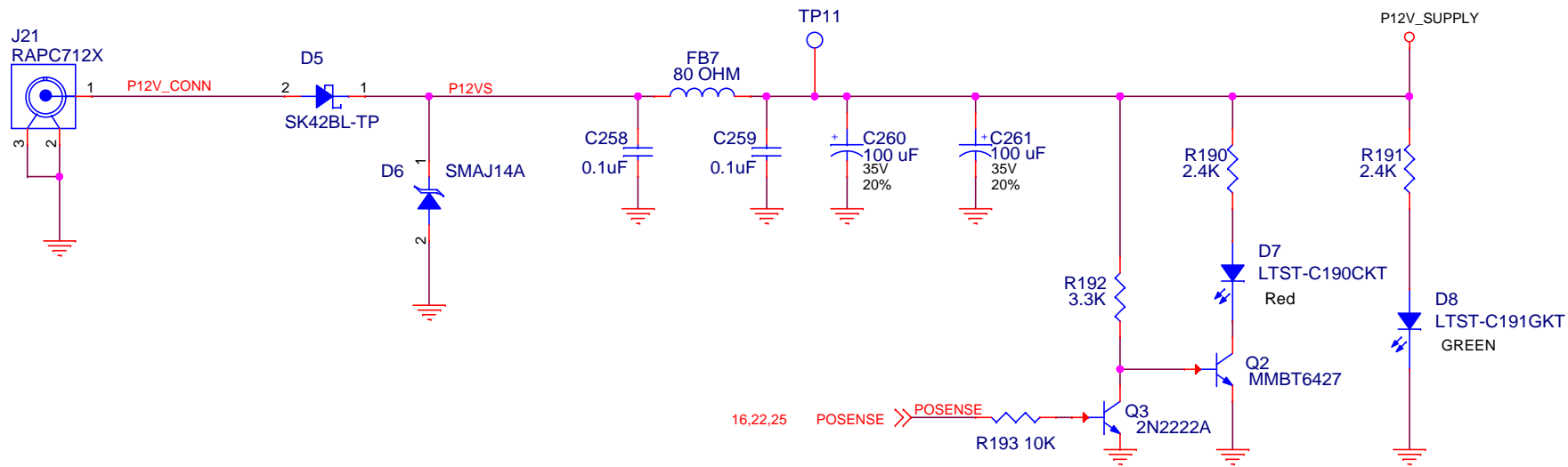
JTAG Boundary scan and Reset

TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	A3	DRAWING NO 2513462		REV D
	ISSUE DATE					
				SCALE		SHEET 19 OF 28

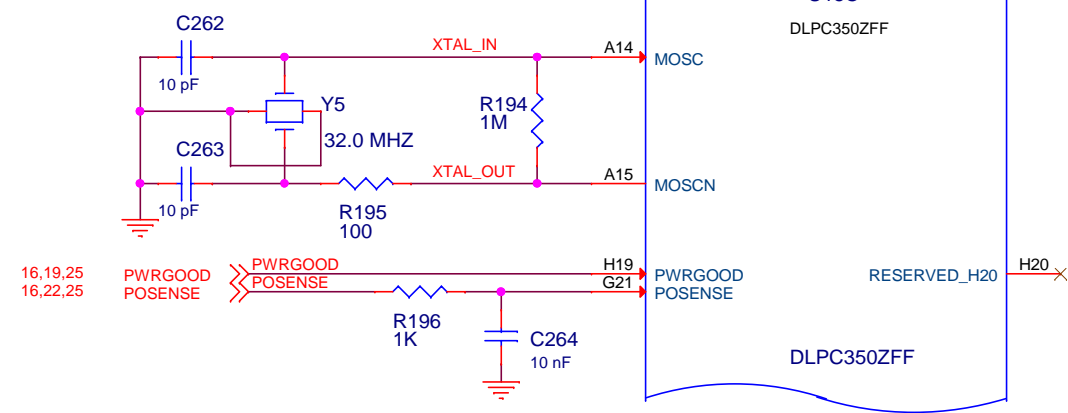


DLPC350 Power and Bypass Capacitors



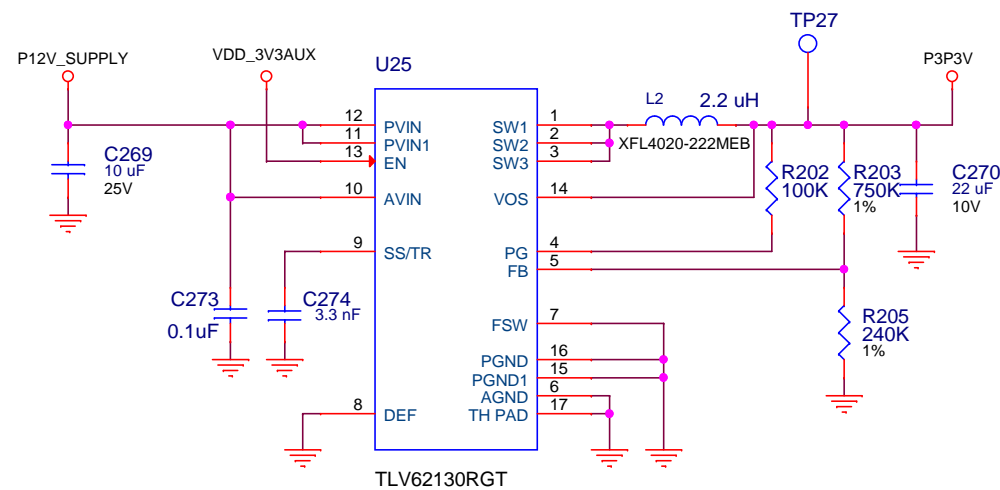
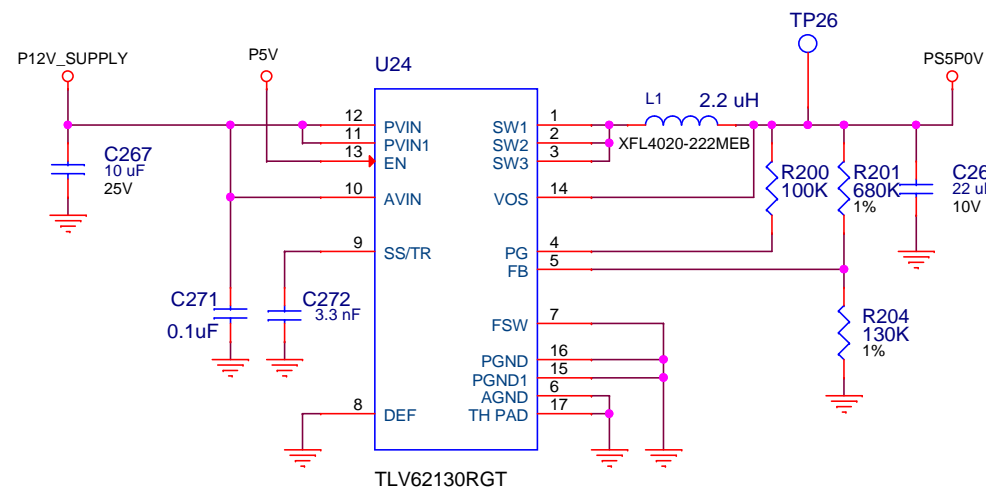
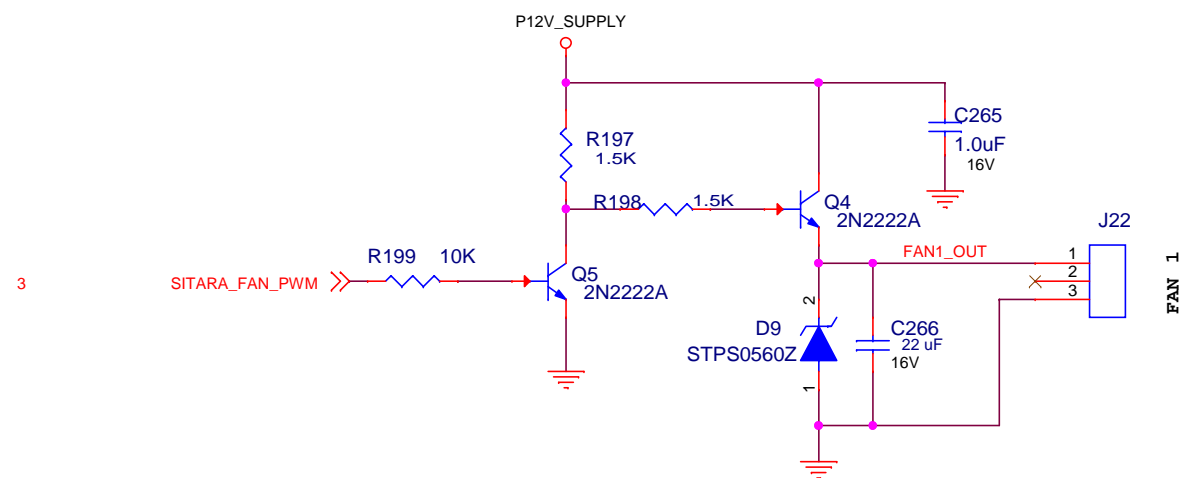


NOTE:
Place crystal circuit and associated
components near DPLC350

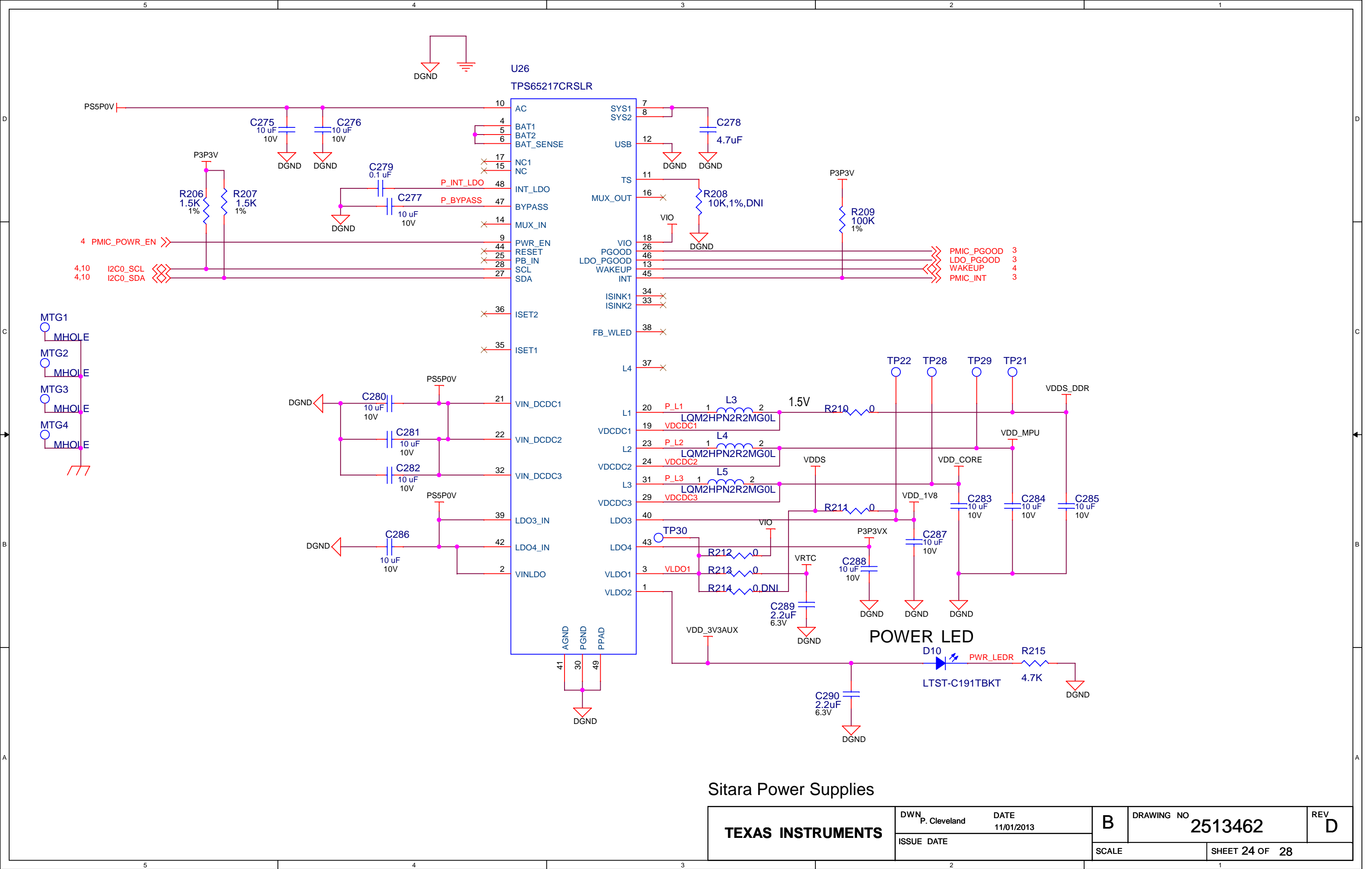


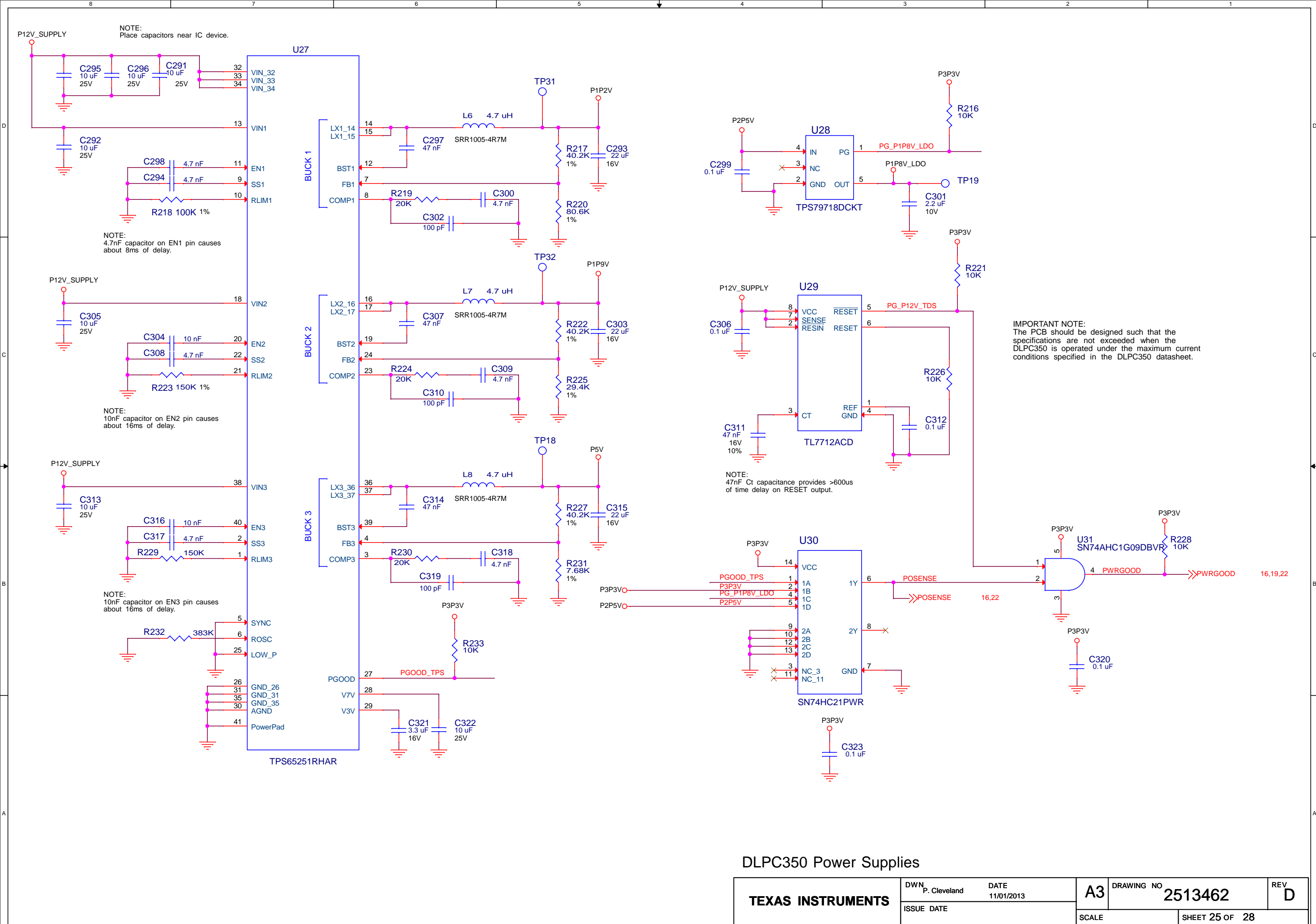
Input Power and Oscillator Input

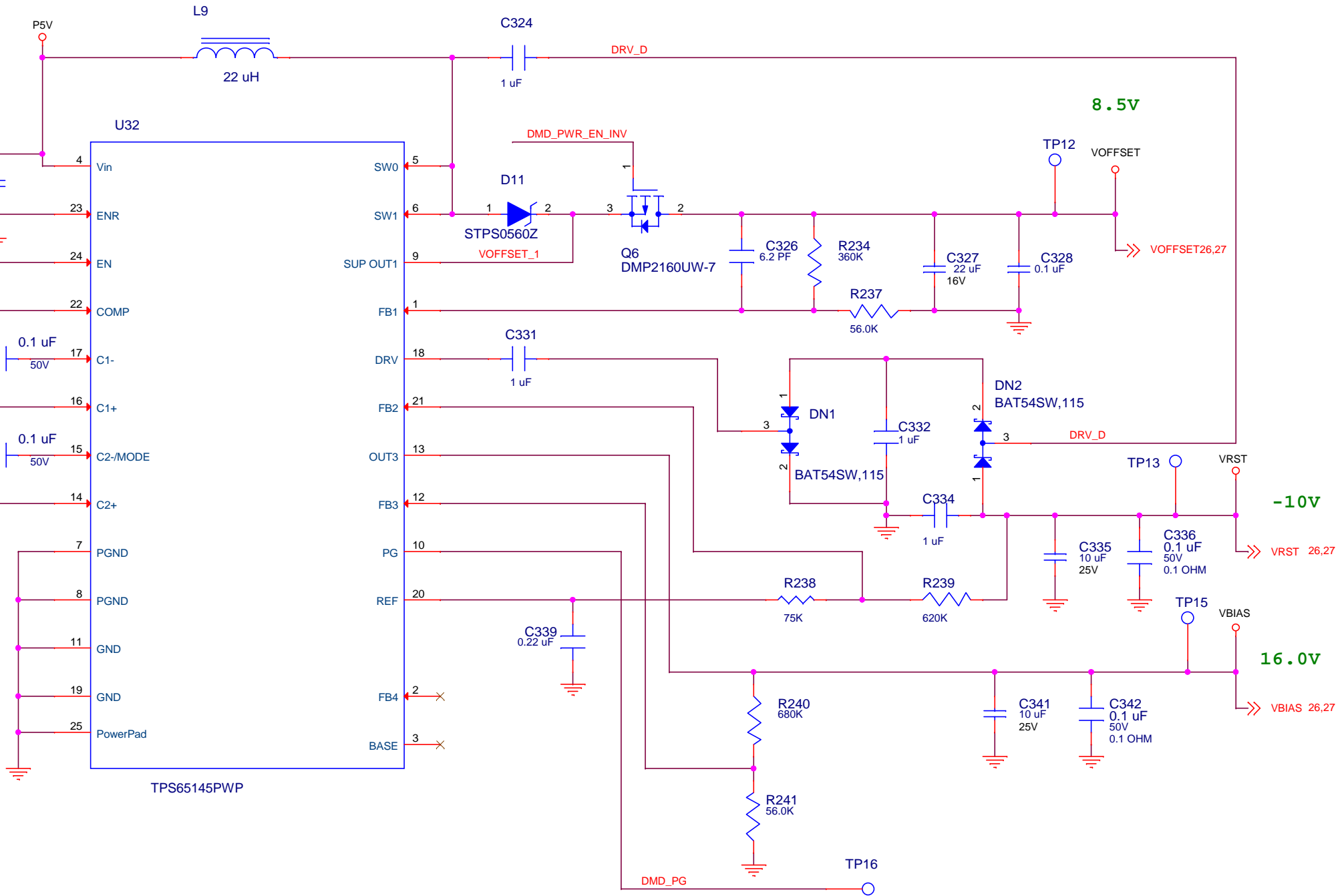
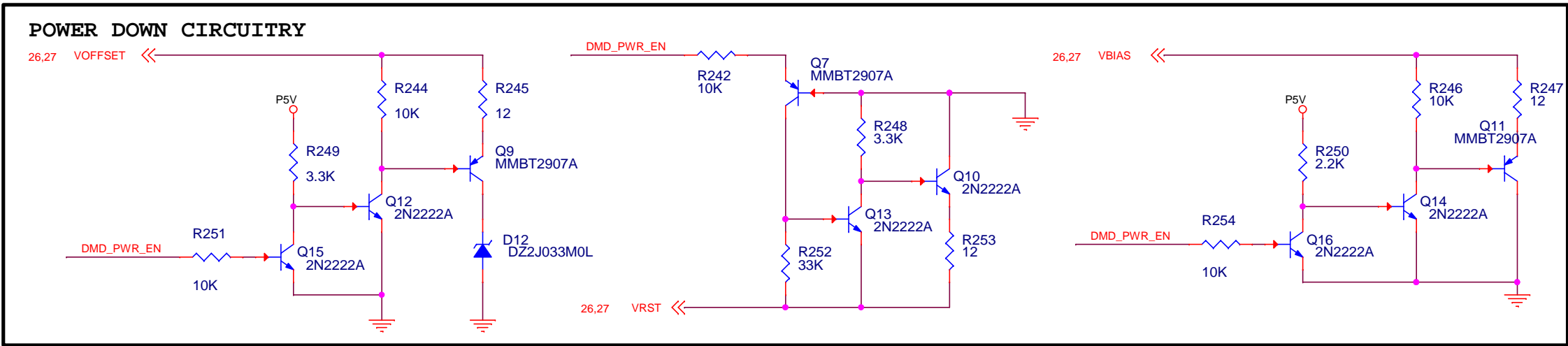
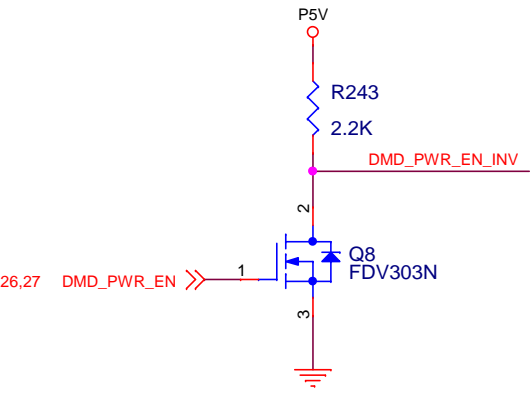
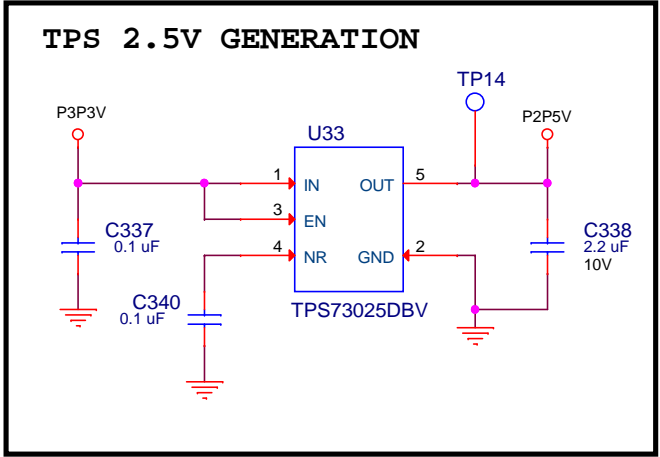
TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	A3	DRAWING NO 2513462	REV D
	ISSUE DATE				
			SCALE	SHEET 22 OF 28	



Fan, 5.0V & 3.3V Power Supplies

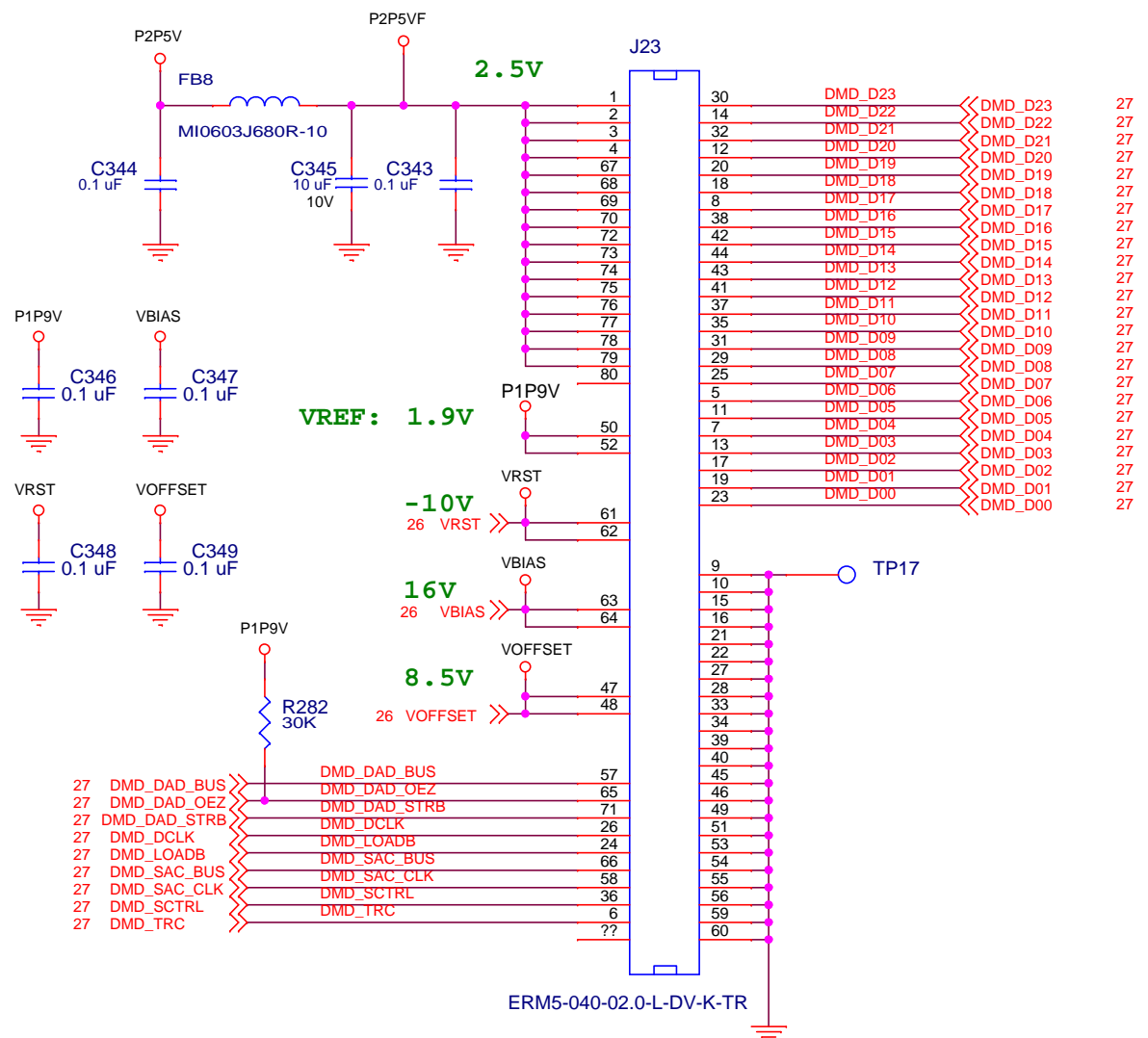






DMD Power Supplies

TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	A3	DRAWING NO 2513462		REV D
	ISSUE DATE					
				SCALE	SHEET 26 OF 28	



SHEET 27 OF 28

Revision History

Rev. - : Draft Release ~ 09/23/2013

Rev. A: Initial Release ~ 11/01/2013

Rev. B: ECO 2138776 Label R32,R36,R208 as DNI, Change R22,R23,R24,R25,R26,R27,R28,R29,R30,R31,R32,R33, R34,R35,R36,R37 value to 10K, Replace U10 with SN74LVC1G17DCK, Disconnect U26-10 from ground, connect to PS5P0V, Disconnect U26-4,5,6 from PS5P0V ~ 01/06/2014

Rev. C: ECO 2139942: Up-date title block, Disclaimer ~ 02/14/2014

Rev. D: ECO 2140608: R157 and R177 are now DNI; Up-dated C350 attributes ~ 03/14/2014

Schematic Revision History

TEXAS INSTRUMENTS	DWN P. Cleveland	DATE 11/01/2013	A3	DRAWING NO 2513462		REV D
	ISSUE DATE					
				SCALE		SHEET 28 OF 28